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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,101	07/18/2003	Guillermo Rozas	TRAN-P072	2896

7590 03/14/2007

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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,101	ROZAS ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 2/8/2007.

Maintained Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-7 and 10-12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Larson (U.S. 5,115,500).

5. As per claim 1:

Larson teaches a method of processing an instruction, said method comprising:

Fetching said instruction using a corresponding address from a memory unit (Larson: Figure 2, column 5 lines 34-67 continued to column 6 lines 1-40)(An instruction is fetched from the I-Store 2 using an address from the memory unit (Instruction Address Register, IAR 3).);

Wherein a plurality of possible meanings are associated with said instruction (Larson: Figure 2, column 5 lines 34-67 continued to column 6 lines 1-40)(There are a possibility of a plurality of meanings for each instruction depending on the concatenated address bits. When an instruction is fetched, it has one of two meanings, which are an

instruction of type 1 if the lower three order bits aren't '111' and an instruction of type 2 if the lower three order bits are '111.');

Concatenating a portion of said corresponding address to said instruction to form an extended instruction, wherein selection of said portion of said corresponding address for said concatenating is independent of region of said memory unit from which said instruction is fetched (Larson: Fig. 2, col. 3, lines 52-64 and col. 5, line 34 to col. 6, line 40)(The selection of the three lower end bits is independent of which region of memory the instruction is fetched from. The three bits are selected to determine how the instruction will be decoded regardless of if the instruction came from the memory units that store type 1 instructions or the memory units that store type 2 instructions.)

And executing said extended instruction, wherein said portion of said corresponding address determines a meaning for said extended instruction from said possible meanings: [The instruction is decoded and then executed with one of the possible meanings, which is dependent on the extended instruction formed from the concatenation. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

6. As per claim 2:

Larson disclosed the method as recited in claim 1 wherein said portion is an address bit (Larson: Fig. 2, col. 5, line 34 to col. 6, line 40).

7. As per claim 3:

Larson disclosed the method as recited in claim 1 wherein said portion is a plurality of address bits (Larson: Fig. 2, col. 5, line 34 to col. 6, line 40).

8. As per claim 5:

Larson disclosed a method of handling an instruction, said method comprising:

Generating said instruction, wherein a plurality of possible meanings are associated with said instruction: [Instructions reside in the I-Store 2 (fig. 2), there are present, therefore they were inherently generated. Each instruction has a plurality of meanings associated with it, dependent on the corresponding address at which it is stored. (Col. 3, lines 15-22, and col. 5, line 34 to col. 6, line 40.)]

Storing said instruction at a particular address in a memory unit such that a portion of said particular address enables determination of a meaning for said instruction from said possible meanings: [Fig. 2, col. 2, lines 21-54 and col. 5, line 34 to col. 6, line 40.]

And before executing said instruction, fetching said instruction using said particular address from am memory unit and concatenating said portion of said particular address to said instruction, wherein selection of said portion of said corresponding address for said concatenating is independent of region of said memory unit from which said instruction is fetched (Larson: Fig. 2, col. 3, lines 52-64 and col. 5, line 34 to col. 6, line 40)(The selection of the three lower end bits is independent of which region of memory the instruction is fetched from. The three bits are selected to determine how the instruction will be decoded regardless of if the instruction came from the memory units that store type 1 instructions or the memory units that store type 2 instructions.)

9. As per claim 6:

Claim 6 essentially recites the same limitations of claim 2. Therefore, claim 6 is rejected for the same reasons as claim 2.

10. As per claim 7:

Claim 7 essentially recites the same limitations of claim 3. Therefore, claim 7 is rejected for the same reasons as claim 3.

11. As per claim 10:

Claim 10 essentially recites the same limitations of claim 1. Therefore, claim 10 is rejected for the same reasons as claim 1.

12. As per claim 11:

Claim 11 essentially recites the same limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

13. As per claim 12:

Claim 12 essentially recites the same limitations of claim 3. Therefore, claim 12 is rejected for the same reasons as claim 3.

New Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 4, 8-9 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (U.S. 5,115,500), in view of ("390 Principles of Operation"), herein referred to as IBM.

16. As per claim 4:

Larson disclosed the method as recited in claim 1.

Larson failed to teach wherein the plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

However, IBM disclosed wherein the plurality of possible meanings include an integer type of instruction and a floating point type of instruction (IBM: Pages 7-1 to 7-6, 9-1 to 9-4, and 9-8 to 9-9)(The combination results in type 1 instructions being the instructions of the IBM 390 ISA. Thus, one of the plurality of possible meanings could be a integer instruction from the 390 ISA or a floating point instruction from the 390 ISA.).

Larson disclosed two separate types of instruction used, but failed to disclose what types of ISA's are used. Since the Larson patent was produced from IBM, one of ordinary skill in the art would have been motivated to look at IBM ISA's for more information on what types of instructions are supported. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the IBM 390 ISA onto the processor of Larson.

17. As per claim 8:

Claim 8 essentially recites the same limitations of claim 4. Therefore, claim 8 is rejected for the same reasons as claim 4.

18. As per claim 9:

Larson is silent on specifically how the instructions are generated and stored in the memory in the specific locations. While Larson describes that high-level programs are compiled before inherently being placed in an instruction memory for execution (Col. 1, lines 11-29), and that the instructions are stored in specific locations so as to define the decoding of the instructions, Larson does not specifically state that the I-Store 2 contains instructions compiled from high-level code, which were generated and stored by use of the compiler. Therefore, while Larson teaches all the actions taken by the compiler, that is, the instructions are generated and stored at specific locations, Larson fails to teach a compiler performs these actions.

However, Examiner takes Official Notice that compilers are used to generate and store instructions in memory, so as to allow programmers to write code in high level languages and allow the compiler to convert and prepare the code for execution by a processor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the generating and storing of the instructions using a compiler since Examiner takes Official Notice compilers are well known in the art and allow programmers to write code in high-level languages instead of machine code.

19. As per claim 13:

Claim 13 essentially recites the same limitations of claim 4. Therefore, claim 13 is rejected for the same reasons as claim 4.

20. As per claim 14:

Claim 14 essentially recites the same limitations of claim 9. Therefore, claim 14 is rejected for the same reasons as claim 9.

Response to Arguments

21. The arguments presented by Applicant in the response, received on 2/8/2007 are not considered persuasive.

22. Applicant argues "Larson doesn't teach or suggest wherein a plurality of possible meanings are associated with said instruction."

This argument is not found to be persuasive for the following reason. There is a plurality of meanings for each instruction depending on the concatenated address bits. When an instruction is fetched, it has one of two meanings, which are an instruction of type 1 if the lower three order bits aren't '111' and an instruction of type 2 if the lower three order bits are '111.' In addition, the claimed limitation doesn't limit the plurality of possibilities to be limited to a single ISA.

23. Applicant argues "Larson doesn't teach or suggest concatenating a portion of said corresponding address to said instruction to form an extended instruction, wherein selection of said portion of said corresponding address for said concatenating is independent of region of said memory unit from which said instruction is fetched."

This argument is not found to be persuasive for the following reason. The selection of the three lower end bits is independent of which region of memory the instruction is fetched from, as these three bits are always selected. The three bits are selected to determine how the instruction will be decoded regardless of if the instruction

came from the memory units that store type 1 instructions or the memory units that store type 2 instructions.

24. Applicant argues "Requesting that the examiner produce art for claim 4 that relied upon official notice in the previous rejection."

The examiner has brought in a new reference that contains both integer and floating-point instructions to read upon claim 4. The applicant requesting prior art for the official notice previously given necessitates the new ground of rejection.

25. Applicant argues "Other methods may be used to generate and store instructions in a memory such as XML and interpreters."

This argument is not found to be persuasive for the following reason. The applicant's use of other examples for techniques to generate and store instructions doesn't disprove that a compiler also generates and stores instructions, which official notice is relied upon as evidence. It doesn't appear that the applicant is requesting prior art that discloses a compiler generating and storing instructions. Thus, the examiner hasn't brought in prior art to teach this limitation and maintains that claim 9 is obvious in light of the official notice given.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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